



FOR ON BOARD 64M DRAM DETECT.
R100 PULL UP '64' LINE. HI->64DRAM LO->16M D-RAM
R101 JUMPER ENABLE CPU CONTROLLED 64 LINE.
R102 JUMPER FOR 16M CHIP. THIS CASE IS NOT USE CPU
CONTROLLED '64' LINE. SO USE THIS JUMPER, YOU MUST
REMOVE R101!!

SOJのRAS,CAS,OEは間違っているので
後で修正すること(回路図のみ)。

まだ回路図のメモが残りません。

CASE FOR 3.3V DRAM, PLACE
IC60, 62
C60, 61, 62, 63

CASE FOR 5V DRAM, PLACE
IB60, 61, 62, 63

CASE FOR 3.3V DRAM, PLACE
IC60, 62
C60, 61, 62, 63

CASE FOR 5V DRAM, PLACE
IB60, 61, 62, 63

REVISION CHECKED 1st EDITION
APPROVED DESIGNED
198-6-11 198-7-9
K.TSURU

AKAI TITLE 8
CIRCUIT NO. L6044801
Design File: C:\WORK\MPC2000\Lab\20477\IMP\6044801
Design Name: (Title)
Schematic Name: main1
Created: Tuesday, July 07, 1998
Modified: Monday, March 01, 1999
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